Optimization of EMI Filters of Multi-Level Flying Capacitor Boost Converter

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***Abstract*—This paper presents the optimization of the EMI filters for a multi-level flying capacitor boost converter (FCBC) by using a frequency-domain EMC model. The objective is to find optimal EMI filters design by estimating the EMI noise on the input and output sides simultaneously. A generic modeling process, suitable for any number of levels, is applied to a three-level flying capacitor boost converter for illustration. The model is developed and validated on an experimental prototype. Then, the filters are designed by an optimization process and validated by measurement. Finally, a sensitivity analysis on the impact of the number of levels and the switching frequency is performed.**

Keywords— Electromagnetic Compatibility, Optimization, Frequency Model, Multi-level Flying Capacitor Boost Converter

I. INTRODUCTION

THE Boost converter is usually needed in renewable energy (RE) systems to raise the low input voltage of renewable energy sources [2], [3] or storage elements as batteries. A major problem for conventional structures is the size of the passive components, especially the input inductor used to store the necessary energy for voltage elevation. Recently, multi-level converters have been widely used in RE applications to decrease the volume of the passive components used in conventional converters. These converters improve efficiency and performance by reducing switching losses and lowering the input voltage ripple [4], [5]. The additional switches in the multi-level DC-DC boost converter also reduce the individual voltage stress on the semiconductor devices. Additionally, higher DC bus voltages can be reached for higher power applications. Although the stress on the semiconductor is less, the multiplication of the number of switching cells leads to more complex EMC (Electromagnetic Compatibility) behavior [6]–[8]. The EN 55011 standard defines the levels of noise allowed on the input and output of the converter, to prevent unacceptable grid pollution in both Differential (DM) and Common Mode (CM). A good understanding of EMC behavior is mandatory for the designers to design appropriate EMC filters. However, sizing EMI (Electromagnetic Interferences) filters is time-consuming using time-domain simulations, and necessitates several iterations. Numerous references address the sizing and optimization of EMI filters, using recursive methods and a primary focus on single-side filtering [9]–[13]. However, designing filters for both sides presents a more complex task due to the non-independence of disturbances from different directions. A method of designing two EMI filters simultaneously by considering the crosstalk between them was proposed in [14], which can solve this problem in the conventional design. This method leads to heavy computation and oversizing of the filters, making it less relevant for optimized converters.

When high power density or lower cost is needed, filter optimization is applied. In this case, the conventional design methodology is insufficient and EMC models dedicated to optimization must be proposed. Ref [15] proposes a conducted emission model for a motor control inverter, combining a lumped parameter circuit with finite-element electromagnetic simulation methods. However, the frequency-domain analysis [16] exhibits very low simulation times, compared to the time-domain and is well adapted to the optimization approach. It replaces the switching devices with equivalent sources, and has already been used in the simple case of a DC-DC converter [17], or drive systems [18]. In [19]–[21], the same method is applied to a three-phase inverter with a resistive load at the output, where only one EMI filter is needed on the input side.

Further studies have been carried out in [22]–[24] on the modeling of power electronics converters from an EMC point of view, with a focus on the converter. Also, in [25], a three-terminal CM EMI model for a UPS has been developed. These works mainly deal with the study of EMI generation and mitigation on the converter's input. This paper aims to design the EMI filters for a multi-level boost converter on both sides. The model is presented and identified in section II and III, in the specific case of 20 kW three-level flying capacitor boost converter. The generalization to n-level is proposed in section IV. Then, in section V, the model is validated in comparison with both experiment and time-domain simulation for a down-scaled power. In Section VI, the filters are designed, optimized, and validated with experimental tests. Furthermore, sensitivity analyses are performed.

This paragraph of the first footnote will contain the date on which you submitted your paper for review, which is populated by IEEE *(Corresponding author: Jean-Luc Schanen.)*

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II. Multi-Level Flying Capacitor Boost Converter Model Parameters Identification

The schematic of the system is shown in Fig. 1. The considered system is a three-level flying capacitor boost converter, which is connected to a 20 kW load, represented by a simple resistance. The duty cycle of each switch is obtained using the well-known boost converter formula.

$$D = 1 - \frac{V_{in}}{V_{out}} \quad (1)$$

In the case of a three-level flying capacitor boost converter, the switches are controlled with 180-degree phase-shift with regard to the switching period. As the result, the inductor current harmonics appear at twice the value of switching frequencies. Also, the flying capacitor C_{fly} is charged up to half of the output voltage in steady-state, what reduces the semiconductor voltage stress. Finally, in the studied topology, to avoid low frequency resonance with the line inductance, the input capacitance C_{in} is split into two parts, including a damping resistance R_{damp} [5].

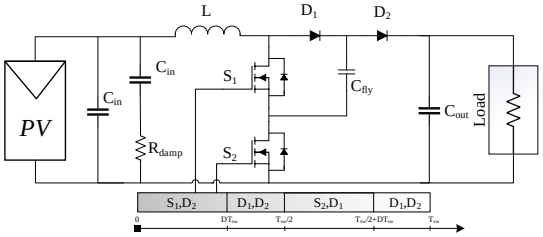


Fig. 1. Schematic of the three-level flying capacitor boost converter.

For the EMC study, a circuit diagram with the parasitic parameters of the system is shown in Fig. 2. Each component including capacitors and inductors are modeled using high frequency model including stray elements. Common mode parasitic capacitors between the power layout and the heatsink (supposed at ground potential) are also represented:

- S_1 MOSFET floating point: C_{AG}
- S_2 MOSFET floating point: C_{CG}
- Minus to the ground: C_{BG}

It is worth noting that the cathode of D_1 and D_2 are also floating points with respect to the ground, but in a first approximation, due to C_{fly} and C_{out} which act as short circuits at high frequency, neglecting the impact of their stray behavior, they have been included in C_{CG} and C_{BG}, respectively. To identify the EMI generation of the considered converter, two LISNs (Line Impedance Stabilization Networks) are used at the input and output of system, to become independent from the PV panels characteristics on the input, or the DC grid characteristic on the output. It should be noticed that the output side could also include a DC-AC converter and be connected to the AC grid, but this paper focuses on the boost converter only.

First of all, the components need to be identified including passive elements and their stray characteristics. These components' values are measured and shown in Table I. Even if some of them are not used in the frequency model (as C_{fly}), all are necessary for the time-domain simulation. In addition, according to [26], C_{pv} is considered to be 100 pF/kW which will be used for validation. However, the influence of this arbitrary value as well as the load parameters is not significant on the results due to the ability of LISNs to stabilize the impedance. In other words, C_{pv} and load are isolated by the LISNs.

TABLE I.
Converter Model Parameters.

L_{Wire} [µH]	1	**C_{out} [µF]**	33
C_{in} [nF]	473	**ESL_{Cout} [nH]**	70
ESL_{Cin} [nH]	60	**ESR_{Cout} [mΩ]**	10
ESR_{Cin} [mΩ]	16	**C_{dec} [nF]**	33
L_b [µH]	146	**ESR_{Cdec} [mΩ]**	10
EPR_{Lb} [kΩ]	25	**C_{fly} [µF]**	20
EPC_{Lb} [pF]	74	**ESL_{Cfly} [nH]**	10
ESR_{Lb}[mΩ]	31	**ESR_{Cfly} [mΩ]**	10
C_{AG_Load} [nF]	0.8	**R_{Load}[mΩ]**	98
C_{BG_Load} [nF]	0.8	**L_{load} [µH]**	11.63

Other key elements to be identified are the stray capacitances to ground brought by the interconnects (C_{AG}, C_{BG} and C_{CG} in Fig. 2). The physical layout of the converter uses a dedicated power module for the three-level flying capacitor boost converter (Fig. 3). The corresponding electrical circuit is given in Fig. 4. The external flying capacitor C_{fly} = 20 µF is connected between points C and D, and an internal capacitor is integrated in the power module. Therefore, these points are equivalent to a short circuit for the capacitive identification. Similarly, B and E points have the same potential at high frequency due to the internal 33 nF decoupling capacitor in the power module. It is worth mentioning that only ESR C_{dec} is used and ESL C_{dec} is neglected due to numerical stability for time simulation, these points are also treated as short circuit for capacitive identification.

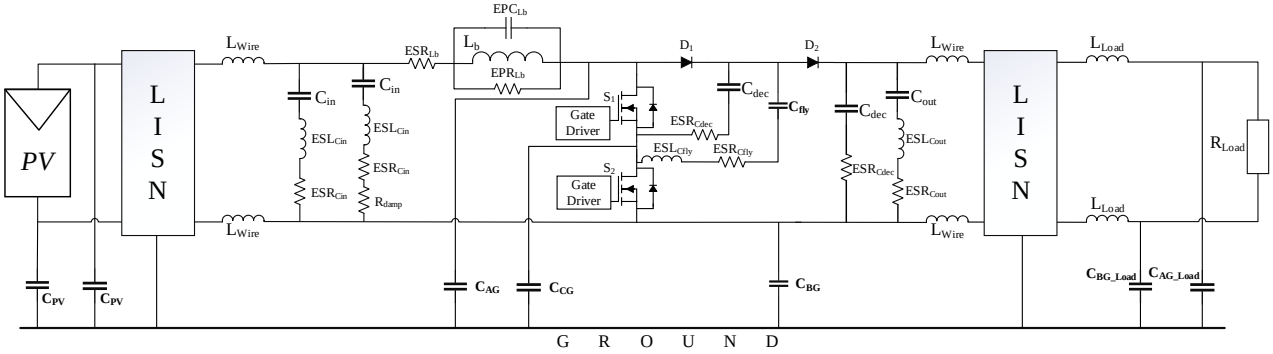


Fig. 2. Schematic of the system with stray elements.

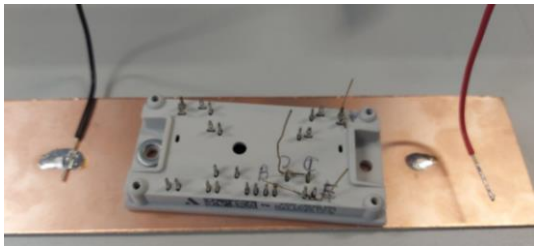


Fig. 3. Dedicated power module to three-level flying capacitor boost converter.

Therefore, the module exhibits only three different points: A (DC bus plus input), B=E (output port and minus DC bus), and C=D (middle point of the FC boost converter), in addition to the ground (module baseplate) G. Due to their quite high value of C_{dec} and C_{oss}, especially at 0 V, it is not feasible to identify each capacitor individually, since they act as high frequency short circuits. Therefore, only the total common mode capacitance has been measured, by connecting the A, B and C points and measuring them with respect to ground.

The measured capacitance is equal to:

$$C_{measured} = C_{AG} + C_{BG} + C_{CG} = 120\ pF \qquad (2)$$

Investigating the internal design of the power module, it was found that the area of the internal layout was almost equal for each potential A, B and C, leading to the assumption of identical values for each of them, thus around 40 pF each.

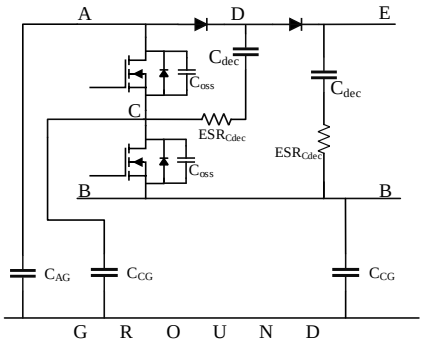


Fig. 4. Three-level boost converter power module.

III. EMC Frequency Model

To obtain the equivalent EMC model, the well-known equivalent source method had been chosen. It replaces the switching devices by equivalent voltage and current sources reproducing the same discontinuities as in the working converter [16]. The value of each source is obtained by its corresponding voltage or current frequency spectrum. However, changing semiconductors into equivalent sources modifies the impedance of all EMC propagation paths, in comparison to the actual switched behavior of the converter. A voltage source is a low impedance in the frequency-domain, and is more compatible with a switch in the ON state than a current source, which is a high impedance. To determine the topology of the equivalent circuit, we decided therefore to identify all possible circuit topologies, by replacing all switches which are turned ON by a voltage source (low impedance, since the switch will be ON after commutation) and all switches which are turned OFF by a current source (high impedance). According to the Boost converter operations (Fig. 1), four different equivalent circuits can be found, summarized in Table II. It is worth noting that Case 2 and Case 4 are similar (both switches OFF and both diodes ON) and obviously give the same equivalent circuit.

TABLE II.
SEMICONDUCTORS STATES IN EACH SWITCHING CASE.

	S_1	D_1	S_2	D_2
Case 1	ON	OFF	OFF	ON
Case 2	OFF	ON	OFF	ON
Case 3	OFF	ON	ON	OFF
Case 4	OFF	ON	OFF	ON

The equivalent circuit of each condition in frequency modeling is then studied. It is worth noting that, for obtaining the equivalent frequency model, the flying capacitor is considered as a pure capacitance and is therefore assumed to be a short circuit in the frequency-domain. This assumption can be made since a high-quality capacitor is integrated internally in the power module, in parallel with the external C_{fly}, resulting in a very low impedance at high frequencies. The other capacitors of the converter (C_{in}, C_{out}) are kept in the frequency model, in order to account for their stray elements. To be noticed that another internal capacitor C_{dec} is added in the power module, in parallel with C_{out}. Both will be taken into account in the frequency model even if the resulting noise will be negligible, due to the high quality of C_{dec}.

In Case 1, S_1 is ON and S_2 is OFF: according to this D_1 and D_2 are respectively OFF and ON. So, by replacing S_1 and D_2 by voltage sources and S_2 and D_1 by current sources, the equivalent circuit of the converter of Fig. 5.a is obtained. The current source replacing D_1 is paralleled with the voltage source replacing S_1 and has therefore no effect on the circuit response. Therefore, it can be removed, and the simplified equivalent circuit is presented in Fig. 5.b.

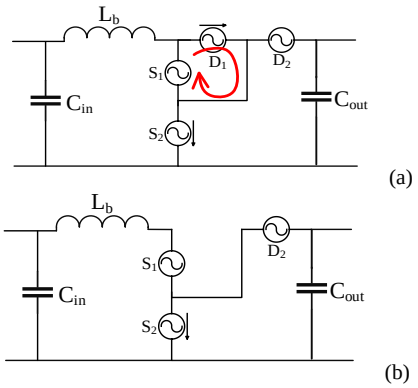


Fig. 5. Converter equivalent circuit in case 1 (a) Complete model (b) Simplified model.

By proceeding in the same way as in this Case 1, the equivalent circuits in other cases listed in Table I are obtained (Fig. 6 and Fig. 7). As explained previously, current sources short circuited by voltage sources are removed (S_1, D_1 in this case, respectively), leading to circuit simplification.

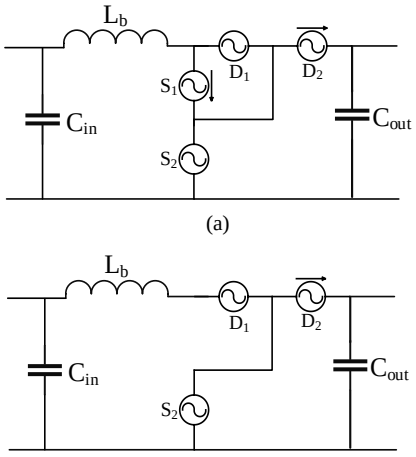
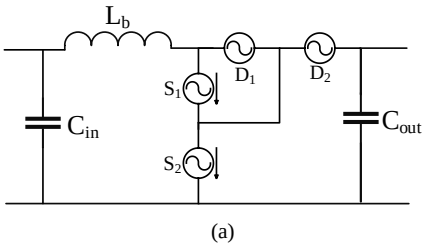


Fig. 6. Converter equivalent circuit in case 3 (a) Complete model (b) Simplified model.



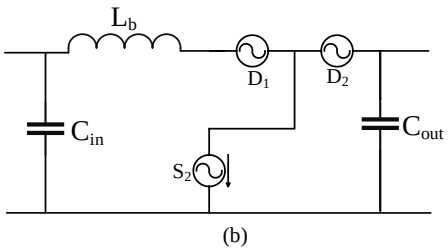


Fig. 7. Converter equivalent circuit in cases 2 and 4 (a) Complete model (b) Simplified model.

Checking three simplified equivalent circuits, it is visible that all of them include two voltage sources and one current source. Also, Fig. 5. b and Fig. 7. b have the same topologies and the only difference with Fig. 6. b is the location of the current source. Therefore, only two possible equivalent circuits in the frequency-domain are obtained which are shown in Fig. 8. To investigate the differences between these two different cases, both will be compared to a time-domain simulation with FFT of the LISN voltage on both input and output.

The values of voltage and current sources shown in Fig. 8 are corresponding to switches voltages or currents in the frequency-domain, derived from the analytical formula using Laplace transform. Time-based information or FFT from the time-domain simulation can be used, as detailed in [27].

Once all elements identified, it was possible to run the time-domain simulations, as well as the two frequency models for comparison purpose. The frequency solving was performed using a homemade tool, and the time-domain simulation run with PSIM software.

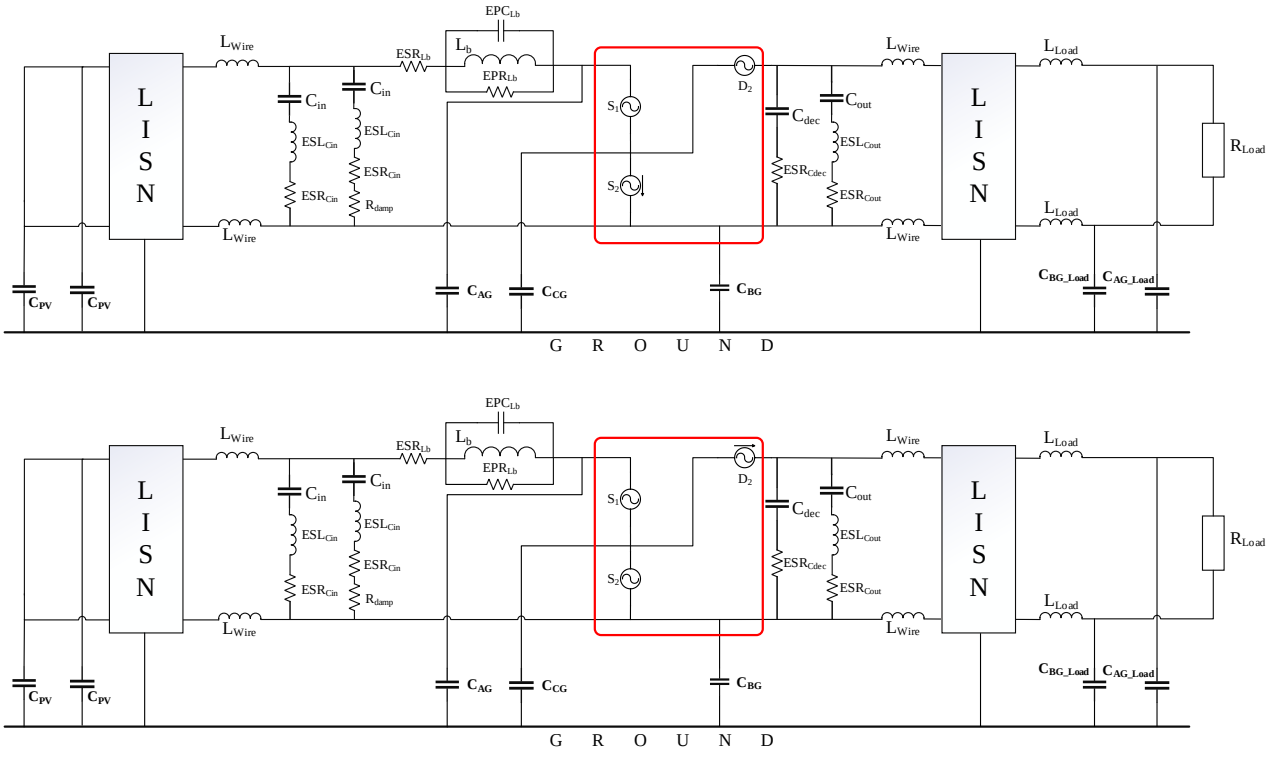


Fig. 8. System equivalent frequency modeling circuit (a) Case 1 (b) Case 2.

Fig. 9 shows the comparison between the two equivalent circuits of Fig. 8.a, Fig. 8.b and the exact time-domain simulation with FFT, for input/output line voltages on input and output LISNs. According to the EMC standards, both sides of the converter need to meet the requirements. therefore, all voltages on each branch of each LISN have to be monitored. The model is therefore checked for all four branches. There is a good matching in the frequency range of interest (10kHz - 3MHz) where EMI filters design process is focused on low frequency part of the spectrum.

There is a peak around 3 MHz that is not modeled in the frequency model. The origin of this peak is an oscillation on the switches' voltages, originated by the resonance between C_{dec} and the stray inductance ESL_{Cout}.

After 3 MHz, there is reduced compatibility between modeling and simulation, which is caused by the assumption of perfect C_{fly}, identification of stray elements, and inaccuracy of sources (rise and fall time not equaling zero). These phenomena have been previously included in the equivalent circuit in literature, but for EMI filter design purposes, they could be initially neglected. In reality, there is no need for accuracy beyond a few megahertz.

From this comparison, both equivalent circuits are comparable. Therefore, we can choose any of them, and we decide to use the one of Fig. 8.a, since it is more suitable for generalization to n-levels, as illustrated in the following section.

IV. Generalization to N-Level

To extend the circuit to multiple levels, a simple approach is followed: each MOSFET in the circuit is replaced with a voltage source, as shown in Fig. 8.a. The diode is represented by a single remaining current source between the bottom MOSFET and the output capacitor. Any other diode currents are internally recycled through the flying capacitors (supposed ideal high frequency short circuits) and do not cause disturbances externally. The equivalent circuit for four levels is illustrated in Fig. 10. In general, with n-levels, there will be n-1 voltage sources and one current source.

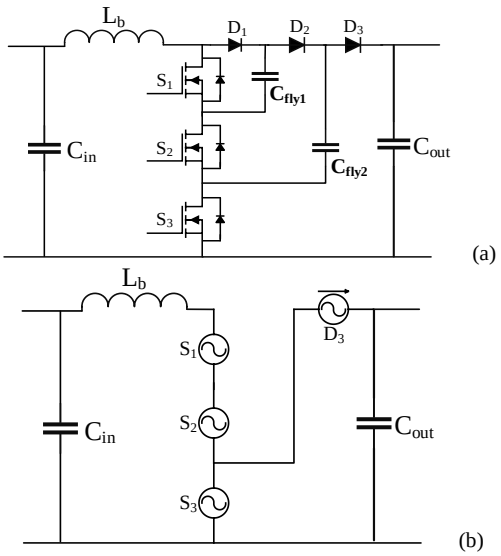


Fig. 10. 4-level flying capacitor boost converter (a) Schematic circuit (b) Equivalent frequency modeling.

V. Model Validation

Based on the EN 55011 standard application, the DC side LISN use 150 Ω common mode termination, whereas it is 5-50 Ω for AC port. Since the output of DC/DC converter is going to be connected to the inverter and an AC grid, it was considered relevant to use the usual 5-50Ω impedance of the CISPR 16 standard for the output side, even if in this paper, the boost converter was connected to a passive load through a LISN. Two phases of this AC LISN (connected on the output side) were used then for the test.

In order to experimentally test the system, high-voltage measurement devices, specifically LISNs, are required. However high voltage LISN were not available in the lab, therefore, it has been decided to test the system at a reduced

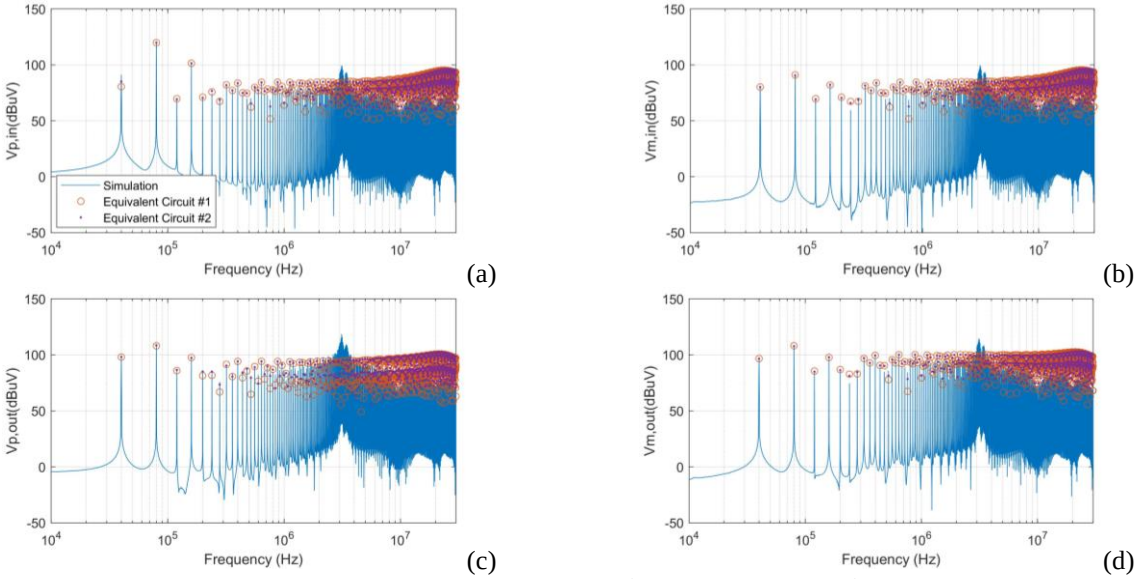


Fig. 9. Model comparison between a) and b) and comparison with the FFT of time-domain simulation for line voltages with respect to the ground. a) Input plus line voltage (Vpin), b) Input minus line voltage (Vmin), c) Output plus line voltage (Vpout), d) Output minus line voltage (Vmout).

voltage of 400 V. It is assumed that the system will operate at the same duty cycle, so the input voltage is considered to be 337 V instead of the original 1180 V (nominal operating voltage of a 1.5 kV PV string as described in [4]).

The configuration of the experimental test prototype is shown in Fig. 11.

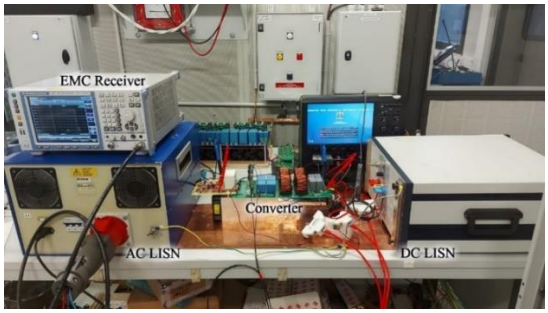


Fig. 11. The experimental setup.

The comparison between experimental and simulation results is shown in Fig. 12. It gives the values of voltages on both input and output LISN branches. Although the global shape looks quite good, the measurement and modeling results show some differences. The low frequency peaks (multiples of the switching frequency up to 1MHz) do not match well for DC plus and DC minus. Since all components were measured with the impedance analyzer, this difference cannot be explained by different component values in experiment and simulation.

A possible reason could be the duty cycle change from the flying capacitor voltage control system, which is not reproduced in the open-loop simulation.

The difference in the high frequency range can be attributed to the effect of stray elements and layout, especially the cabling between the LISN and the converter, which are not accurately accounted for in the modeling.

Also, the resonance around 3 MHz seen in Fig. 9 is more damped in reality than in simulation, so it is not visible in Fig. 12.

Finally, although there are some differences when each peak is considered, the envelope of the measured and modeled spectra are almost the same, and the model can be validated for being used in the filter design process.

VI. EMI Filter Design by Optimization

A. *Filter Design*

After establishing the equivalent circuit that has helped understanding the root cause of noise propagation, this circuit can also be used to design the CM and DM filters using an optimization process. This process will be detailed in this section.

The considered standards, EN 55011, for 20 kW application have defined the limits and required amount of noise attenuation that EMI filters must provide which is shown in Fig. 13. As mentioned earlier, the AC standard has been chosen for output side even if the load was a DC resistance.

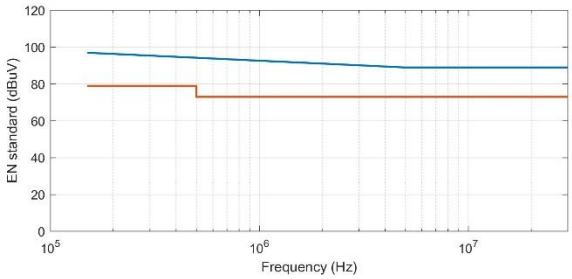


Fig. 13. Disturbance voltage limits (quasi-peak) according to EN 55011, A: DC (input) standard, B: AC (output).

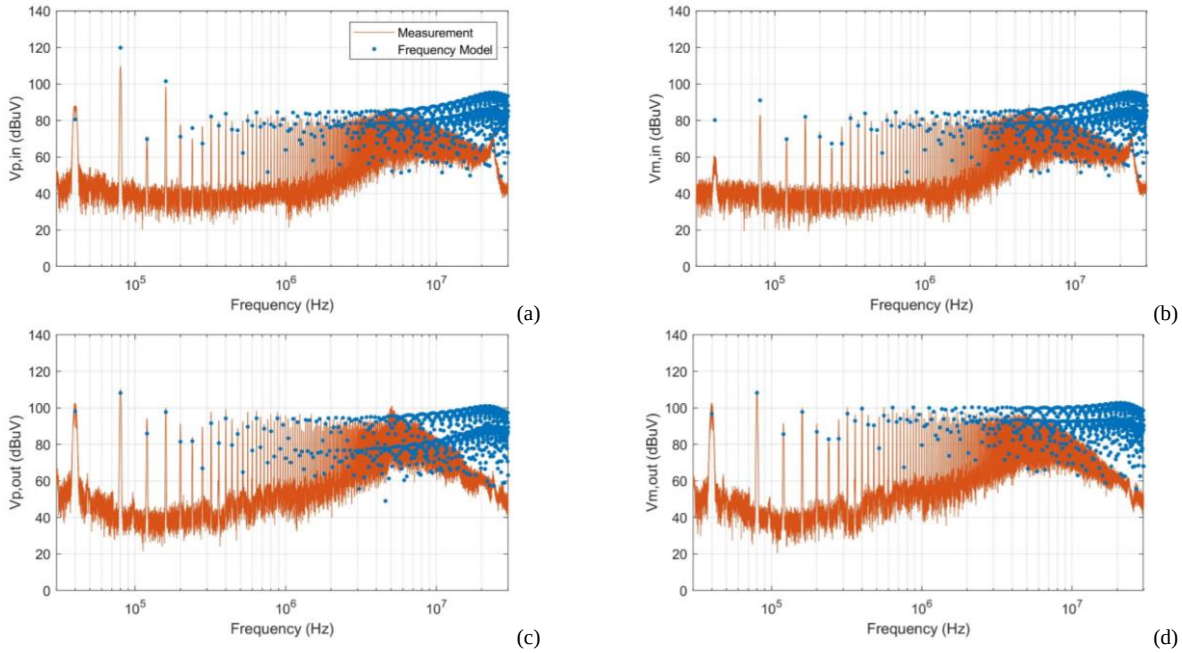


Fig. 12. Experimental and time-domain simulation comparison for line voltages. a) Input plus line voltage (Vpin), b) Input minus line voltage (Vmin), c) Output plus line voltage (Vpout), d) Output minus line voltage (Vmout).

To attenuate conducted EMI noise in compliance with EMI standards, it is usually necessary to add EMI filters to the system. Consisting of magnetic components such as CM chokes and DM inductors, these EMI filters are often large and cumbersome and can represent a significant portion of the system's total weight. It is therefore necessary to obtain the appropriate selection of EMI filter components in addition to regulatory compliance.

Sizing those filters based on conventional design process choosing the cut-off frequency of the EMI filters necessitates several iterations, since the disturbances on both sides are not independent, which leads to heavy computation and oversizing of the filters. Also, as it does not guarantee an optimal result, it is not relevant for the optimization approach. In this case, the conventional design methodology is insufficient and EMC (Electromagnetic Compatibility) models dedicated to optimization must be proposed.

Optimization selects a set of design variables to achieve the best solution (objective function) from all feasible solutions (constraints). The volume of the filter components is considered as the objective function. Fig. 14 shows the schematic of the system in the presence of the EMI filters on both sides. Since the standard is defined for both sides, two filters are considered in the first step.

Unlike the approach taken in [9], where the value of inductance is assumed as a design variable in the optimization process, the filter values in this study are modified by adjusting the technological parameters descripting the inductor (core size, turn number), and the value of capacitances C_x and C_y. This allows directly taking into account the sizing constraints and evaluating the volume more precisely.

The inductor is modeled based on the model proposed in [28] using the core and wire dimensions. The design variables are core dimensions and turn number. The volume of the inductor (Vol_L) is calculated as follows:

$$Vol_L = \pi * (R_{ext} + d_s)^2 * (H + 2d_s) \quad (3)$$

R_{ext}, d_s and H are the external radius of the core, wire diameter and height of core, respectively.

The capacitor volume models are based on manufacturer datasheet interpolation. EMC filter capacitors, which are specialized components for EMC applications, are considered from KEMET® company. These capacitors serve different purposes depending on their class. Class X capacitors are specifically designed for line-to-line usage and provide protection against differential mode interference. On the other hand, Class Y capacitors are intended for line-to-ground applications and offer protection against common mode interference. According to the IEC 60384-14 standard, industrial applications typically require X_1 and Y_1 class capacitors, while general purpose applications commonly use X_2 and Y_2 classes. It is also possible to substitute one class with another in certain cases. For instance, for class X_1, classes Y_1 or Y_2 can be used as substitutes. However, when it comes to class Y_1, there are no viable substitutions available [29].

Based on the manufacturer proposal, R41 and P295 capacitor types are chosen for Cx and Cy application respectively. Fig. 15 and Fig. 16 illustrate the volume interpolation of these specific capacitors according to the datasheet. The R^2 index is the linear correlation coefficient that represents the proportion of the variance and indicates the quality of the curve fitting. A value closer to one indicates better curve fitting.

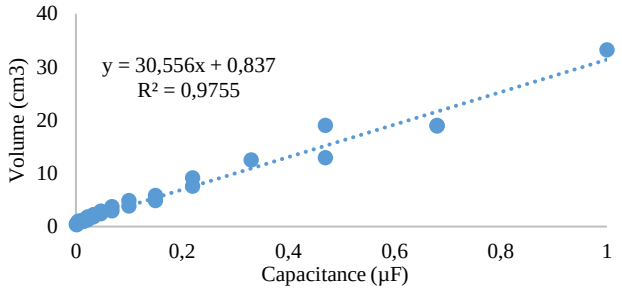


Fig. 15. C_x capacitor volume interpolation.

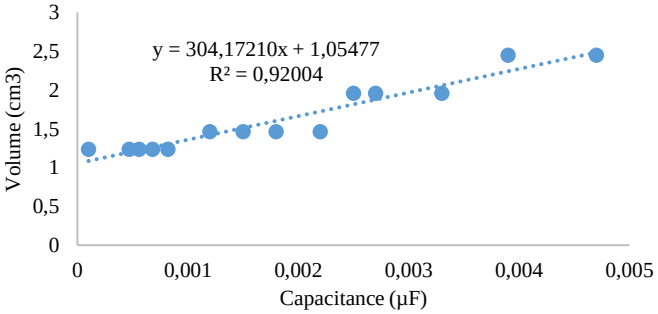


Fig. 16. C_y capacitor volume interpolation.

Furthermore, the optimization process must satisfy some constraints. Two kinds of constraints are involved: EMC constraint which is defined to meet the standards, but also design constraints, such as saturation of magnetic materials, filling area for inductors, etc.

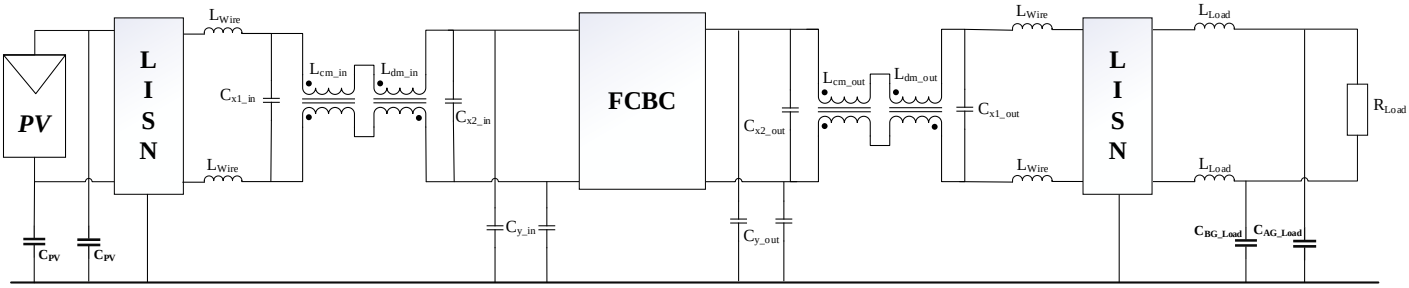


Fig. 14. Structure of the studied EMI filters with its equivalent circuit.

In the case of design constraints, the rule generally followed is to limit the conductor's current density (J) to 6 A/mm² depending on the cooling conditions. Furthermore, the peak flux density should stay below a certain value to avoid core saturation. The peak flux density is below B_{max} = 0.2 for Epcos N30 ferrite cores. This type of core has both high permeability and low drop permeability at high frequencies, making it suitable for EMI approaches. The peak value of flux density is obtained by expanding Faraday law in the frequency model as following:

$$B = \frac{1}{NS}\int V_L dt \quad (4)$$

V_L is calculated by sum of its harmonics in switching frequency which is obtained by frequency analysis as (5):

$$V_L = \sum_{i=1}^{k} V_{module}(i)\cos(\omega_i t + \varphi_i) \quad (5)$$

The V_L waveform is evaluated from the frequency model of the converter. It accounts for the real operating point of the common mode inductor. By replacing eq (5) in (4), the peak value of flux density is calculated by eq. (6).

$$B_{max} = \frac{1}{NS}\sqrt{\sum_{i=1}^{k}\left(\frac{V_{module}(i)}{\omega_i}\right)^2} \quad (6)$$

k is the number of voltage harmonics that should be considered reasonable to have a correct evaluation of the peak value. In [30], it is shown that the flux density is almost due to the first harmonic. So, maximum frequency is chosen to be 40 kHz which corresponds to the switching frequency.

It is worth noting that permeability drop with frequency can be taken into account in the model. However, as flux density is almost related to low frequencies and in these frequencies the permeability drop is negligible, this phenomenon has been neglected for peak flux density computation.

The EMC constraints are linked to the standards defined for 150 kHz to 30 MHz. Several issues can be encountered during optimization since changing input parameters can have opposite roles on different part of the EMC spectrum. Therefore, it was decided to focus on the harmonic that requires the most attenuation. So, the EMC constraints have been reduced to one single frequency which is the lowest frequency and has the greatest impact on the volume of the filter. Of course, the high frequency range behavior of the spectrum should be verified after optimization. This is normally not an issue due the high attenuation of the filter in high frequency range. However, the impact of the stray elements and the permeability drop can deteriorate the attenuation. This will be discussed later in this paper.

The block diagram of the optimization strategy is shown in Fig. 17. The EMC generation uses a combination of the LISN, filter and converter models solved in the frequency-domain, using a dedicated tool (Cades software), suitable for optimization. Indeed, it computes the results quickly and provides the gradients for the optimization algorithm (Jacobian and even Hessian if needed). Note that the gradient algorithm requires derivable models.

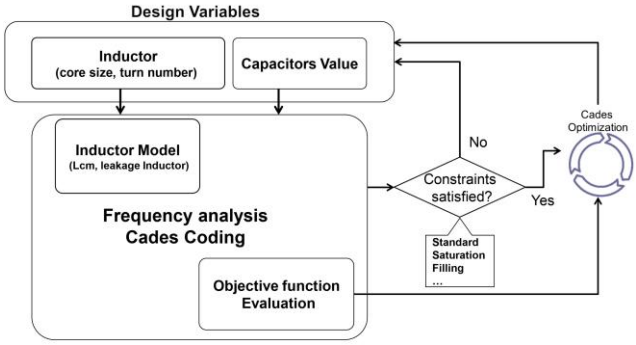


Fig. 17. Block diagram the implemented optimization strategy.

To sum up, the whole system including LISNs and filters (Fig. 14) is modeled, and the objective function is the total volume of the two filters. In addition to constraints applied to magnetics (filling factor, saturation, …). EMC constraints have been applied to each voltage branch of each LISN. It is to be noted that this methodology does not uses the usual DM/CM decomposition method.

Applying gradient optimization as a strategy, some parts of the filters are going toward the minimum boundaries, what means they are useless. Therefore, after optimization, it was found that no C_y and no C_x were necessary in the output filter, and no C_{x1_in} on the input filter. The best configuration within the constraints is obtained as shown in Fig. 18. The value of each component and its manufacturing requirements are listed in Table III.

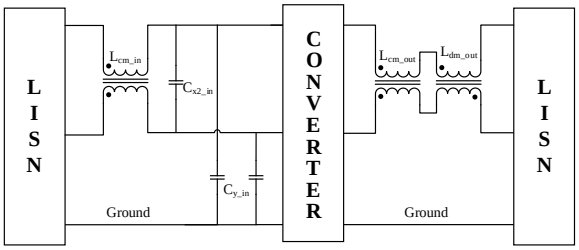


Fig. 18. Optimal filters configuration for the rated power.

TABLE III.
EMC OPTIMIZED FILTER PARAMETERS FOR THE RATED POWER.

Components	Value
L_{cm_in} [mH]	0.36
L_{cm_out} [mH]	0.46
L_{dm_out} [µH]	60
C_{x_IN} [µF]	2.22
C_{y_IN} [nF]	23.5

With the developed frequency-domain models, the effect of applying the mentioned filter to the system is shown in Fig. 19. The comparison is made for two cases. The first case (blue) is considered as a fixed inductance and the second (orange) case has been carried out by assigning the permeability drop based on datasheet. The second case is interpolated to 4 MHz due to lack of data for higher frequencies. However, the higher frequencies are not related to electrical phenomena and are dominated by filter leakage and layout. As can be seen, this design meets the standards, although the inductances are affected by the permeability drop, what validates again the design by optimization methodology.

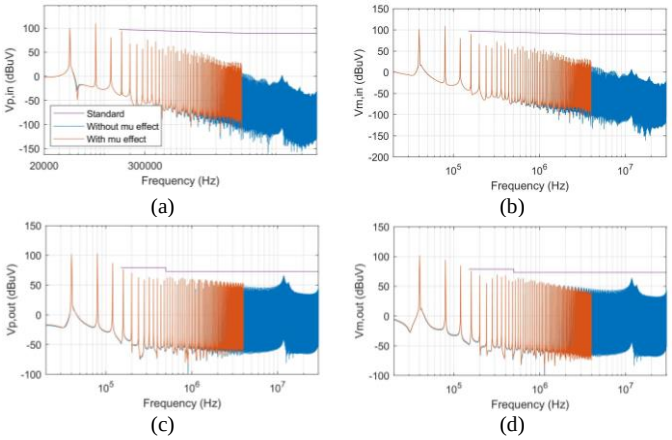


Fig. 19. Noises with optimal designed filters for the rated power. a) Input plus line voltage (Vpin), b) Input minus line voltage (Vmin), c) Output plus line voltage (Vpout), d) Output minus line voltage (Vmout).

As explained in Section V, due to the unavailability of high-voltage measurement equipment, a different operating point was chosen for the experimental verification of the system. By optimizing the system for reduced power operation, a new configuration for the filters was obtained (shown in Fig. 20). This new configuration eliminates the need for a differential mode choke. For this application, X2 and Y2 capacitors were selected that are suitable for general purpose and lower voltage applications. The Y2 capacitor, designated R41 with the same specifications as in the previous optimization, was selected. The X2 capacitors were selected as KEMET R46 capacitors. The volume interpolation of this capacitor type, based on the data sheet, is shown in Fig. 21. The optimization results are shown in Table IV.

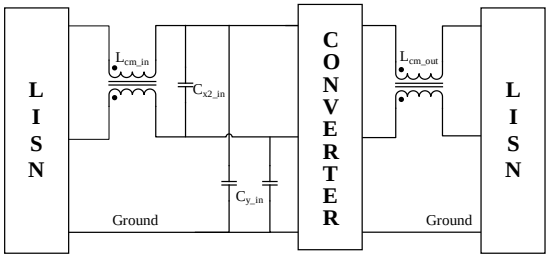


Fig. 20. The optimal filters configuration for Vout=400 V.

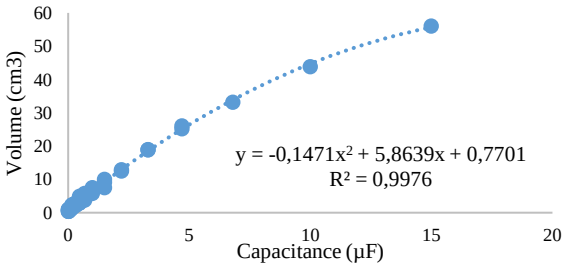


Fig. 21. R46 capacitor volume interpolation.

TABLE IV.
EMC OPTIMIZED FILTER PARAMETERS FOR THE REDUCED POWER.

Components	Value
L_{cm_in} [mH]	0.24
L_{cm_out} [mH]	1.67
C_{x_IN} [µF]	0.33
C_{y_IN} [nF]	10

The result of applying the optimized filter to the down-scaled system is shown in Fig. 22. The redesigned filters also have good performance as the rated power case.

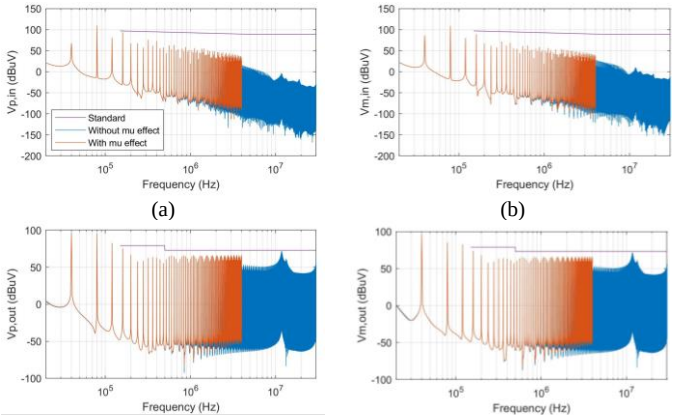


Fig. 22. Noises with optimal designed filters for the reduced power. a) Input plus line voltage (Vpin), b) Input minus line voltage (Vmin), c) Output plus line voltage (Vpout), d) Output minus line voltage (Vmout).

B. *Experimental Results*

Fig. 23 and Fig. 24 show the implemented filters for the rated and the reduced power, respectively. In production, an effort is made to keep the components as close together as possible to avoid high series inductance. For the same reason, no holes are used in the boards and all components are soldered in SMD. The power layouts for both input and output filters are quite simple, using the back of the PCB as a ground plane to connect the C_y capacitors in the most direct way.

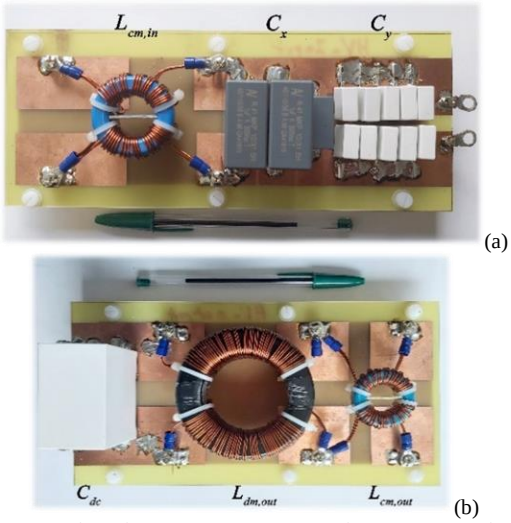


Fig. 23. EMI filter for rated power: (a) input filter, (b) output filter.

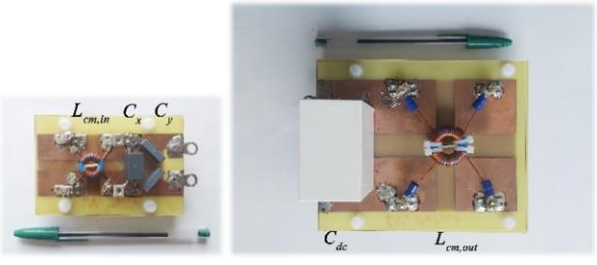


Fig. 24. EMI filter for the reduced power: (a) input filter, (b) output filter.

The experimental setup with the filters is shown in Fig. 25. To reduce the ESL between the filters and the converter, they are connected as close as possible to each other. It should also be noted that the filter layout on the output side also supports the DC output capacitor, which was not part of the design process (white block on the left Fig. 23. b and Fig. 24. b).

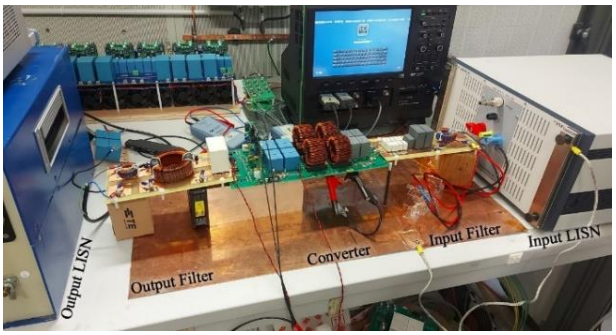


Fig. 25. Experimental setup with the rated power filters.

Fig. 26 and Fig. 27 show the results of experiments and simulations for a reduced power test. Fig. 26 focuses specifically on the results obtained using the filter designed for rated power, while Fig. 27 shows the results when the reduced filter is used. In the case of the rated filter (Fig. 26), it exceeds the requirements because it is designed for full power and is therefore considered overdesigned for reduced power. As a result, the spectrum is largely below the standard.

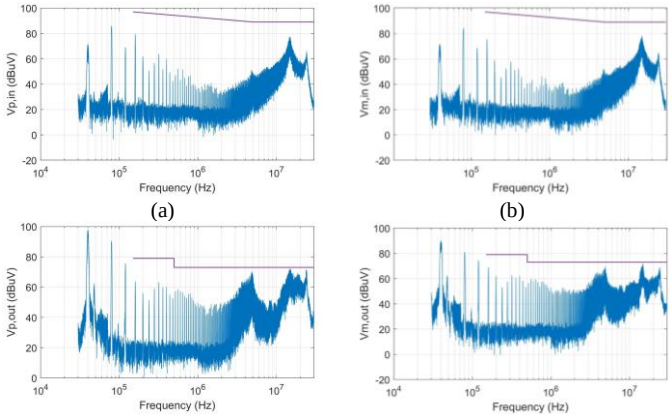


Fig. 26. Experimental and simulation comparison in the case of reduced power with rated filters. a) Input plus line voltage (Vpin), b) Input minus line voltage (Vmin), c) Output plus line voltage (Vpout), d) Output minus line voltage (Vmout).

In the case of reduced filters (Fig. 27), where the filters are designed on the basis of reduced power, the filters are correctly designed. There is also some overpass at the output side in the high frequency range, which is related to stray elements and layout, and should be considered in the manufacturing process.

Also, the input noise on the input side does not reach its limit due to the interaction. However, the values of the input filters cannot be reduced because the resulting output noise would exceed the standard.

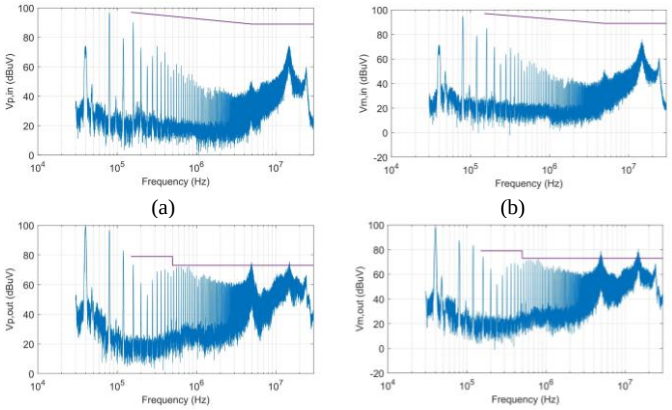


Fig. 27. Experimental and simulation comparison in the case of reduced power with reduced filters. a) Input plus line voltage (Vpin), b) Input minus line voltage (Vmin), c) Output plus line voltage (Vpout), d) Output minus line voltage (Vmout).

C. Impact of the number of levels and the switching frequency on EMC volume

Once validated in the case of a three-level topology, the method can now be used to investigate the effect of key design parameters of the converter, as the number of levels or the switching frequency to check the effect of the parameters on the EMC filter volume. This is examined in the following section.

- *Effect of the number of levels*

The generic EMC representation of the multi-level boost converter defined in Section IV is used for this purpose. For each number of levels, the sources are expressed analytically in the Laplace domain, and the optimization process is run to obtain the optimal volume of EMI filter for different number of levels (Fig. 28). The switching frequency is kept fixed at 40 kHz. As presented, there is no specific trend in changing the number and each topology should be evaluated by itself. For a better conception, the value of each component for EMI filters is listed in Table V.

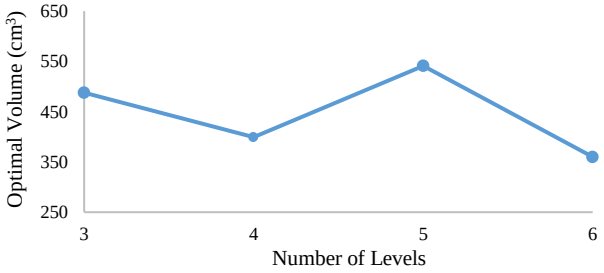


Fig. 28. Optimal volume of EMI filter for different number of levels.

TABLE V.
THE VALUE OF THE EMI FILTERS COMPONENTS FOR DIFFERENT NUMBER OF LEVELS.

	Level Number	3	4	5	6
	Volume [cm³]	488	399	541	360
Input Filter	Lcm_in [mH]	0.315	-	0.379	0.196
	Cx2_in [uF]	1.98	-	1.97	0.382
	Cy_in [nF]	31.4	18.1	46	36.7
Output Filter	Lcm_out [mH]	1.65	2.07	1.79	1.33
	Ldm_out [mH]	0.141	0.14	0.154	0.106

Changing the number of levels causes the harmonics in the frequency to shift. For example, the critical harmonic, which is used in the design process, is the first peak in a 5-level application (160 kHz), while it is the second peak in a 3-level application (160 kHz=2*80kHz). It is important to note that the effective harmonic in n-level flying capacitor boost converters is defined by (n-1)*fsw, where in this case, it is 80 kHz and 160 kHz for 3-level and 5-level, respectively.

To have better discussion on the results, the noises values for 3-level and 5-level are listed in Table VI at 160 kHz which is the first harmonic in the frequency range of the standard. Comparing the 3-level and 5-level noises, the value of the noise at this frequency on the input side (including common mode and differential mode) is almost the same, but the output common mode noise of the 5-level is higher than that of the 3-level. This makes sense of the small difference between the optimum value of total EMI filters in these two applications (481 cm^3 vs 541 cm^3). This comparison can be repeated for conditions with four and six levels. However, it is not included in this paper to avoid repetition. In conclusion, it can be seen that there is no global trend for changing the number of levels, since they all change together.

TABLE VI.
COMMON AND DIFFERENTIAL MODE VOLTAGES FOR DIFFERENT NUMBER OF LEVELS AT 160 KHZ

	3-Level	5-Level
CMV,in [dBµV]	105	105
DMV,in [dBµV]	113	113
CMV,out [dBµV]	108	111.5
DMV,out [dBµV]	100	101

- *Switching frequency effect*

The optimal volume of EMI filter for a 3-level flying capacitor boost converter for different switching frequencies is shown in Fig. 29.

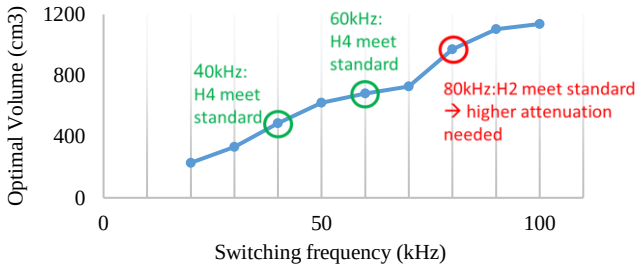


Fig. 29. Optimal volume of EMI filter for different switching f requencies.

Studying Fig. 29, there are some thought-provoking points. First, an incremental trend by switching frequency increase and another is a jump between 70 to 80 kHz. The jump happens because the critical harmonic changes. Before 70 kHz as the switching frequency, the fourth harmonic of the spectrum -280kHz- is the main harmonic above 150 kHz, and it is used for designing EMI filters. However, after 80 kHz, the second harmonic of the spectrum -160kHz- becomes significant in the design process as it enters the standard range. Since the amplitude of the disturbance source at 160 kHz is higher than the one at 280 kHz, the filter attenuation for 80 kHz switching frequency must be higher than the one needed for 70 kHz, resulting in higher volume. Fig. 30 illustrates the impact of optimal EMI filters on the system at three different switching frequencies. The fourth harmonic of the spectrum is subject to constraints for 40 and 60 kHz switching frequencies, while it is the second harmonic for 80 kHz switching frequency. This phenomenon has already been explained in [28].

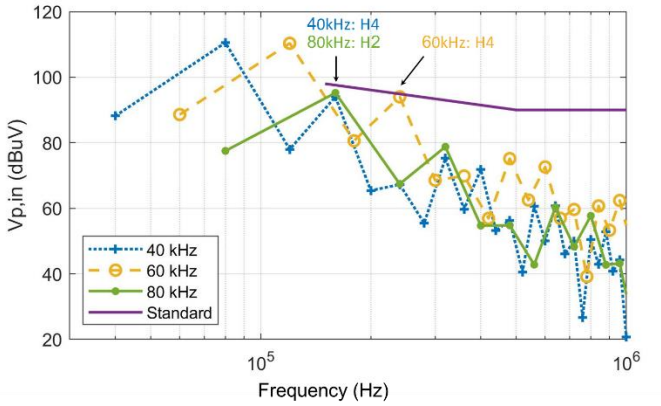


Fig. 30. The effect of optimal EMI filters for different switching frequencies (Analytical Model).

On the other hand, based on [28] due to the shift of the critical harmonic with frequency, the optimal weight of the EMI filter should decrease with frequency because the cut-off frequency of the filter should increase. However, Fig. 29 shows an opposite behavior. This is due to the fact that EMI filters are simultaneously designed on both sides of the converter. Indeed, table VII shows that values of the input filter are decreasing with switching frequency, confirming the results of [28], but at the same time it is noticed that the output filter is bigger what leads to the increase of the total volume.

TABLE VII.
THE VALUE OF THE EMI FILTERS COMPONENTS FOR DIFFERENT SWITCHING FREQUENCIES.

	Frequency	40 kHz	60 kHz
Input Filter	Lcm_in [mH]	0.315	0.209
	Cx2_in [uF]	1.98	0.717
	Cy_in [nF]	31.4	23.1
Output Filter	Lcm_out [mH]	1.65	2.58
	Ldm_out [mH]	0.141	0.246

To investigate this behavior, Table VIII shows the amplitude of the EMC noise at the first frequency appearing in the frequency range of the standard. For 40 kHz, this switching frequency, it is 160 kHz (harmonic 4), for 60 kHz, it is 240 kHz, because harmonic 3 (180 kHz) is of very low amplitude, due to the intrinsic behavior of the 3-levels converter. These results show that actually the output noise is increased with 60 kHz switching frequency whereas it is decreased for the input side. This phenomenon cannot be forecasted without the optimization strategy.

TABLE VIII.
COMMON AND DIFFERENTIAL MODE VOLTAGES AT DIFFERENT SWITCHING FREQUENCY

Switching Frequency	**40 kHz**	**60 kHz**
CMV,in [dBµV]	105	98.5
DMV,in [dBµV]	113	105.5
CMV,out [dBµV]	108	111
DMV,out [dBµV]	100	106.5

Finally, considering these studies, it can be noted that the best value of the EMI filters can be changed from case to case and there is no specific rule for the EMI filters design. This highlights the importance of optimization, which is the main focus of this study.

VII. Conclusions

In this paper, the frequency model of a three-level flying capacitor boost converter has been presented. The process of obtaining the frequency model is very generic and can be applied to any number of levels. The identification methods of the sources and stray elements were explained. The model was validated by both experimental and time-domain simulation, focusing on the low frequency part of the spectrum (below 3 MHz). The EMI filters on both sides were considered and designed simultaneously using an optimization strategy. The optimized filters were built and tested. The noises were attenuated according to the requirements of the standards. Finally, some sensitivity analysis on number of levels and switching frequency have been performed which highlighted the importance of optimization.

References

[1] M. Tadbiri-Nooshabadi, J.-L. Schanen, H. Iman-Eini, and L. G. A. Rodrigues, "Frequency Model for EMC Study of Multi-Level Flying Capacitor Boost Converter," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2023, pp. 3677–3683. doi: 10.1109/ECCE53617.2023.10362484.

[2] H. Watanabe, K. Kusaka, K. Furukawa, K. Orikawa, and J. Itoh, "DC to single-phase AC Voltage Source Inverter with power decoupling circuit based on flying capacitor topology for PV system," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 1336–1343. doi: 10.1109/APEC.2016.7468041.

[3] A. N. Kasiran, A. Ponniran, M. A. Harimon, and H. H. Hamzah, "A Study of 4-level DC-DC Boost Inverter with Passive Component Reduction Consideration," *J. Phys. Conf. Ser.*, vol. 995, no. 6, p. 012062, Apr. 2018, doi: 10.1088/1742-6596/995/1/012062.

[4] H. Keyhani and H. A. Toliyat, "Flying-capacitor boost converter," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 2311–2318, 2012, doi: 10.1109/APEC.2012.6166145.

[5] G. Perez, L. G. Alves Rodrigues, and A. Bier, "Full-SiC Flying Capacitor Boost Converter for 1500 v multi-string PV inverter," *2021 23rd Eur. Conf. Power Electron. Appl. EPE 2021 ECCE Eur.*, pp. 1–10, 2021, doi: 10.23919/epe21ecceeurope50061.2021.9570532.

[6] M. Liu, J. Liu, and X. Wang, "An Intuitive and Accurate EMI Model for a Modular Multilevel Converter," in *2020 IEEE International Conference on Information Technology,Big Data and Artificial Intelligence (ICIBA)*, Nov. 2020, pp. 1337–1342. doi: 10.1109/ICIBA50161.2020.9276914.

[7] S. Tiwari, S. Basu, T. M. Undeland, and O. M. Midtgard, "Efficiency and Conducted EMI Evaluation of a Single-Phase Power Factor Correction Boost Converter Using State-of-the-Art SiC Mosfet and SiC Diode," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7745–7756, 2019, doi: 10.1109/TIA.2019.2919266.

[8] S. Kumar, S. K. Voruganti, B. Akin, and G. Gohil, "Common-Mode Current Analysis and Cancellation Technique for Dual Active Bridge Converter Based DC System," *IEEE Trans. Ind. Appl.*, vol. 58, no. 4, pp. 4955–4966, 2022, doi: 10.1109/TIA.2022.3173895.

[9] A. Singh, A. Mallik, and A. Khaligh, "A Comprehensive Design and Optimization of the DM EMI Filter in a Boost PFC Converter," *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2023–2031, 2018, doi: 10.1109/TIA.2018.2789859.

[10] L. Ravuri and S. Lukic, "A Comprehensive Approach towards Multi-Objective EMI Filter Design Optimization in High-Frequency SiC-based Motor Drives," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, pp. 1692–1697, 2022, doi: 10.1109/APEC43599.2022.9773762.

[11] H. Movagharnejad and A. Mertens, "Design Methodology for Dimensioning EMI Filters for Traction Drives with SiC Inverters," *2021 23rd Eur. Conf. Power Electron. Appl. EPE 2021 ECCE Eur.*, pp. 1–10, 2021, doi: 10.23919/epe21ecceeurope50061.2021.9570678.

[12] K. Nomura, "Density-based Topology Optimization for Conductor Design of EMI filters with Improved Impedance Boundary Condition," *IEEE Int. Symp. Electromagn. Compat.*, vol. 2022-Septe, pp. 377–382, 2022, doi: 10.1109/EMCEurope51680.2022.9901191.

[13] G. Liu, J. Zhang, J. Yuan, J. Yang, W. Gao, and Q. Yang, "Electromagnetic Protection Optimization of the Intelligent Electronic Devices Based on the Passive EMI Filter Design," *5th IEEE Conf. Energy Internet Energy Syst. Integr. Energy Internet Carbon Neutrality, EI2 2021*, pp. 2448–2453, 2021, doi: 10.1109/EI252483.2021.9713149.

[14] J. Zhang, W. Chen, Y. Sha, Y. Han, and X. Yang, "EMI filter analysis for transformer-less photovoltaic inverter," *2016 IEEE 8th Int. Power Electron. Motion Control Conf. IPEMC-ECCE Asia 2016*, pp. 1556–1560, 2016, doi: 10.1109/IPEMC.2016.7512523.

[15] A. Safayet and M. Islam, "Modeling of Conducted Emission for a Three-Phase Motor Control Inverter," *IEEE Trans. Ind. Appl.*, vol. 57, no. 2, pp. 1202–1211, 2021, doi: 10.1109/TIA.2021.3052744.

[16] B. Revol, J. Roudet, J.-L. Schanen, and P. Loizelet, "EMI Study of Three-Phase Inverter-Fed Motor Drives," *IEEE Trans. Ind. Appl.*, vol. 47, no. 1, pp. 223–231, Jan. 2011, doi: 10.1109/TIA.2010.2091193.

[17] M. Delhommais, G. Dadanema, Y. Avenas, F. Costa, J. L. Schanen, and C. Vollaire, "Design by optimization of power electronics converter including EMC constraints," in *2016 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, Sep. 2016, pp. 182–187. doi: 10.1109/EMCEurope.2016.7739226.

[18] B. Touré, J.-L. Schanen, L. Gerbaud, T. Meynard, J. Roudet, and R. Ruelland, "EMC Modeling of Drives for Aircraft Applications: Modeling Process, EMI Filter Optimization, and Technological Choice," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1145–1156, Mar. 2013, doi: 10.1109/TPEL.2012.2207128.

[19] W. Zhou, Y. Yao, and X. Chen, "EMI Modeling Method and Active Suppression Technology of Common-Mode Electromagnetic Interference in Three-Phase Two-Level Inverter Based on Four-Bridge Topology," *IEEE Trans. Ind. Appl.*, vol. PP, pp. 1–11, 2024, doi: 10.1109/TIA.2024.3360368.

[20] Y. Xiang, X. Pei, W. Zhou, Y. Kang, and H. Wang, "A Fast and Precise Method for Modeling EMI Source in Two-Level Three-Phase Converter," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10650–10664, Nov. 2019, doi: 10.1109/TPEL.2019.2891120.

[21] W. Zhou, X. Pei, Y. Xiang, and Y. Kang, "A New EMI Modeling Method for Mixed-Mode Noise Analysis in Three-

Phase Inverter System," *IEEE Access*, vol. 8, pp. 71535–71547, 2020, doi: 10.1109/ACCESS.2020.2983084.

[22] D. O. Boillat, F. Krismer, and J. W. Kolar, "EMI Filter Volume Minimization of a Three-Phase, Three-Level T-Type PWM Converter System," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2473–2480, Apr. 2017, doi: 10.1109/TPEL.2016.2617085.

[23] Z. Shen, D. Jiang, T. Zou, and R. Qu, "Dual-Segment Three-Phase PMSM with Dual Inverters for Leakage Current and Common-Mode EMI Reduction," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5606–5619, 2019, doi: 10.1109/TPEL.2018.2866338.

[24] A. Nidhal, C. Dhia, and S. Lassad, "Modelling of conducted EMI generated by a three-phase PWM rectifier," in *2017 International Conference on Green Energy Conversion Systems (GECS)*, Mar. 2017, pp. 1–4. doi: 10.1109/GECS.2017.8066163.

[25] S. Ohn *et al.*, "Three-terminal common-mode EMI model for EMI generation, propagation, and mitigation in a full-sic three-phase ups module," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8599–8612, Sep. 2019, doi: 10.1109/TPEL.2018.2883714.

[26] Ó. López *et al.*, "Eliminating Ground Current in a Transformerless Photovoltaic Application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, Mar. 2010, doi: 10.1109/TEC.2009.2037810.

[27] M. T. Nooshabadi, J.-L. Schanen, S. Farhangi, and H. Iman-Eini, "Frequency Model for EMI Study of Three-Phase Grid Connected Photovoltaic Inverter on Both DC and AC Sides," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2023, pp. 620–625. doi: 10.1109/APEC43580.2023.10131388.

[28] M. Delhommais, G. Dadanema, Y. Avenas, J. L. Schanen, F. Costa, and C. Vollaire, "Using design by optimization for reducing the weight of a SiC switching cell," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016, pp. 1–8. doi: 10.1109/ECCE.2016.7855545.

[29] Kemet, "Safety Capacitors Overview."

[30] A. Mujezinović, E. Turajlić, A. Alihodžić, M. M. Dedović, and N. Dautbašić, "Calculation of Magnetic Flux Density Harmonics in the Vicinity of Overhead Lines," *Electronics*, vol. 11, no. 4, p. 512, Feb. 2022, doi: 10.3390/electronics11040512.